



STIC EIC 2100 Search Request Form

122785
99

Today's Date:

5-24-04

What date would you like to use to limit the search?

Priority Date: 12-11-00

Other:

Name C Britt

AU 2133 Examiner # 78678

Room # 4A12 Phone 308 2391

Serial # 10/016863

Format for Search Results (Circle One):

PAPER

DISK

EMAIL

Where have you searched so far?

USP DWPI EPO JPO ACM IBM TDB

IEEE INSPEC SPI Other _____

Is this a "Fast & Focused" Search Request? (Circle One) YES NO

A "Fast & Focused" Search is completed in 2-3 hours (maximum). The search must be on a very specific topic and meet certain criteria. The criteria are posted in EIC2100 and on the EIC2100 NPL Web Page at <http://ptoweb/patents/stic/stic-tc2100.htm>.

What is the topic, novelty, motivation, utility, or other specific details defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract, background, brief summary, pertinent claims and any citations of relevant art you have found.

Method to reduce the number of addresses stored
after memory test (no scan)

Detect faulty memory address

Compare 1st detected address with a 2nd
(fail) detected address

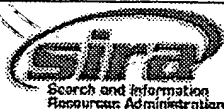
See flow chart fig 2
+ claim 1

STIC Searcher David Holloway

Phone 308-7772

Date picked up 5-24-04

Date Completed 5-25-04



DIALOG 417³⁸

31 min

Examiner Britt:

Attached please find the results of your search request re: Mehtod to reduce the number of addresses stored after memory test....I don't think I found much of use. There were a few hits on removal of duplicate addresses, but not in an error correcting environment.

David Holloway
308-7794

| Set | Items | Description |
|------|--|---|
| S1 | 3748381 | CORRUPT? OR BAD OR FAULT? OR ERROR? OR FAIL? OR FLAW? OR - DEFECT? |
| S2 | 1409564 | ADDRESS? OR LOCATION? |
| S3 | 1618880 | MEMOR? OR STORAGE? OR RAM OR SRAM OR ROM OR PROM OR EPROM - OR EEPROM |
| S4 | 7109767 | TEST? OR CHECK? OR VERIF? OR VALID? |
| S5 | 9024700 | COMPAR? OR MATCH? OR IDENTIC? OR SAME? OR DUPLICAT? |
| S6 | 3340 | (REMOV? OR REPLAC? OR REJECT? OR DISCARD?) (2N) (DUPLICAT? OR SAME? OR IDENTICAL?) |
| S7 | 19 | S1 AND S2 AND S6 |
| S8 | 166 | S2 AND S6 |
| S9 | 166 | S8 AND (S3 OR S4 OR S5) |
| S10 | 35 | S8 AND S3 AND (S4 OR S5) |
| S11 | 12 | S10 AND (REDUC? OR SAVE? OR COMPACT? OR LESS OR FEWER?) |
| S12 | 26 | S10 AND (DETECT? OR FIND? OR LOCAT? OR IDENTIF?) |
| S13 | 48 | S7 OR S11 OR S12 |
| S14 | 31 | RD (unique items) |
| S15 | 27 | S14 NOT PY>2000 |
| File | 8: Ei Compendex(R) 1970-2004/May W3 | (c) 2004 Elsevier Eng. Info. Inc. |
| File | 35: Dissertation Abs Online 1861-2004/Apr | (c) 2004 ProQuest Info&Learning |
| File | 65: Inside Conferences 1993-2004/May W4 | (c) 2004 BLDSC all rts. reserv. |
| File | 2: INSPEC 1969-2004/May W3 | (c) 2004 Institution of Electrical Engineers |
| File | 94: JICST-EPlus 1985-2004/May W1 | (c) 2004 Japan Science and Tech Corp (JST) |
| File | 111: TGG Natl. Newspaper Index (SM) 1979-2004/May 25 | (c) 2004 The Gale Group |
| File | 233: Internet & Personal Comp. Abs. 1981-2003/Sep | (c) 2003 EBSCO Pub. |
| File | 6: NTIS 1964-2004/May W4 | (c) 2004 NTIS, Intl Cpyrght All Rights Res |
| File | 144: Pascal 1973-2004/May W3 | (c) 2004 INIST/CNRS |
| File | 434: SciSearch(R) Cited Ref Sci 1974-1989/Dec | (c) 1998 Inst for Sci Info |
| File | 34: SciSearch(R) Cited Ref Sci 1990-2004/May W3 | (c) 2004 Inst for Sci Info |
| File | 99: Wilson Appl. Sci & Tech Abs 1983-2004/Apr | (c) 2004 The HW Wilson Co. |
| File | 95: TEME-Technology & Management 1989-2004/May W2 | (c) 2004 FIZ TECHNIK |

15/5/1 (Item 1 from file: 8)
DIALOG(R) File 8: Ei Compendex(R)
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05544153 E.I. No: EIP00045151531

Title: Efficient method of eliminating inclusion overhead in snoop-based CC-NUMA systems

Author: Suh, Hyo-Joong; Yoo, Seung Wha; Jhon, Chu Shik

Corporate Source: Seoul Natl Univ, Seoul, S Korea

Source: IEICE Transactions on Information and Systems v E83-D n 2 2000. p 159-167

Publication Year: 2000

CODEN: ITISEF ISSN: 0916-8532

Language: English

Document Type: JA; (Journal Article) Treatment: G; (General Review)

Journal Announcement: 0006W3

Abstract: In a Cache Coherent Non-Uniform **Memory** Access (CC-NUMA) system, **memory** transactions can be classified into two types: inter-node transactions and intra-node transactions. because the latency of inter-node transactions is usually hundreds times larger than that of intra-node transactions, it is important to **reduce** the latency of inter-node transactions. Even though the remote cache in the CC-NUMA systems improves the latency of inter-node transactions through caching the remote **memory** lines, the remote and processor caches of snoop-based CC-NUMA systems have to retain the multi-level cache inclusion property for the simplification of snooping. The inclusion property degrades the cache performance by following factors. First, all the remote **memory** lines in a processor cache should be preserved in the remote cache of the **same** node. Second, a line replacement at the remote cache **replaces** the **same address** line in the processor caches, which does not comply with the replacement policy of the processor caches. In this paper, we propose Access-list which renders the inclusion property unnecessary, and evaluate the performance of the proposed system by program-driven simulation. From the simulation results, it is shown that the miss rates of caches are **reduced** and the efficiency of the snoop filtering is similar to the system with the inclusion property. It turns out that the performance of the proposed system is improved up to 1.28 times. (Author abstract) 16 Refs.

Descriptors: Buffer **storage** ; Information retrieval systems; Network protocols; Multiprocessing systems; Computer simulation; Data processing; Performance

Identifiers: Cache coherent non uniform **memory** access; Internode transactions; Snoopy protocol

Classification Codes:

722.1 (Data Storage, Equipment & Techniques); 903.3 (Information Retrieval & Use); 723.5 (Computer Applications); 722.4 (Digital Computers & Systems); 723.2 (Data Processing)

722 (Computer Hardware); 903 (Information Science); 723 (Computer Software)

72 (COMPUTERS & DATA PROCESSING); 90 (GENERAL ENGINEERING)

15/5/10 (Item 4 from file: 2)

DIALOG(R)File 2:INSPEC

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4732295 INSPEC Abstract Number: B9409-1265B-049, C9409-5210B-017

Title: Circuit structure relations to redundancy and delay

Author(s): Saldanha, A.; Brayton, R.K.; Sangiovanni-Vincentelli, A.L.

Author Affiliation: Cadence Design Syst. Inc., San Jose, CA, USA

Journal: IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems vol.13, no.7 p.875-83

Publication Date: July 1994 Country of Publication: USA

CODEN: ITCSDI ISSN: 0278-0070

U.S. Copyright Clearance Center Code: 0278-0070/94/\$04.00

Language: English Document Type: Journal Paper (JP)

Treatment: Theoretical (T); Experimental (X)

Abstract: The existence of redundant stuck- **faults** in a logic circuit is potentially detrimental to high-speed operation, especially when there are false paths that are longer than the circuit delay. Keutzer, Malik, and Saldanha (KMS) in IEEE transactions of Computer Aided Design, vol. 10, no. 4, p. 427, April 1991 have proved that redundancy is not necessary to reduce delay by presenting an algorithm that derives an equivalent irredundant circuit from a given redundant circuit, with no increase in delay. The KMS algorithm consists of an iterative loop of timing analysis, gate **duplications**, and redundancy **removal** to successively eliminate long false paths. In this paper we resolve the main bottlenecks of the KMS algorithm by providing an efficient single-pass algorithm to simultaneously remove all long false paths from a given circuit. We achieve this by relating a circuit structure property based on path lengths to the testability (redundancy) and delay. The application of this algorithm to a variety of related logic synthesis problems is described. (21 Refs)

Subfile: B C

Descriptors: combinatorial circuits; delays; **fault location**; iterative methods; logic CAD; logic testing; redundancy

Identifiers: circuit structure relations; logic circuit design; delay; redundant stuck- **faults**; logic circuit; high-speed operation; false paths; circuit delay; algorithm; equivalent irredundant circuit; redundant circuit; KMS algorithm; iterative loop; timing analysis; gate duplications; redundancy removal; long false paths; single-pass algorithm; circuit structure; path lengths; testability; logic synthesis problems

Class Codes: B1265B (Logic circuits); B1130B (Computer-aided circuit analysis and design); C5210B (Computer-aided logic design); C7410D (Electronic engineering)

15/5/21 (Item 6 from File: 6)

DIALOG(R)File 6:NTIS

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0123795 NTIS Accession Number: AD-657 247/XAB

Self-Repair Techniques Investigation

(Rept. no. 4, 1 Jun 66-31 May 67 (Final))

Cole, F. B. ; Zimmerman, S. E.

Westinghouse Electric Corp Baltimore Md Surface Div

Corp. Source Codes: 375520

Report No.: MDE-2566; ECOM-02343-F

Aug 67 108p

Journal Announcement: USGRDR6720

Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.

NTIS Prices: PC A06/MF A01

Contract No.: DA-28-043-AMC-02343(E); DA-1P0-20401-A327; 1P0-20401-A327-03-04

The report describes a set of techniques which can be used to design and construct self-repairing digital systems with spare parts switching. Both the problem of **fault detection** and **location** and the problem of spare switching are discussed. Residue coding for arithmetic unit **fault detection** and **location** is discussed and **rejected**. Then, **duplication** techniques for both **fault location** and repair are discussed. A design plan is given for a demonstration model to demonstrate self-repair techniques. The design plan includes logic equations, timing diagrams, and a detailed operational description. Finally, recommendations are made for future efforts. (Author)

Descriptors: Digital systems; Maintenance; Coding; Reliability; **Errors** ; Computer logic; Relaxation oscillators; Logic circuits; Data **storage** systems

Identifiers: **Error** -correcting codes; Computer hardware; Self-repairing systems

Section Headings: 62A (Computers, Control, and Information Theory--Computer Hardware)

| Set | Items | Description |
|-----|---------|---|
| S1 | 37722 | CORRUPT? OR BAD? |
| S2 | 491701 | ADDRESS? OR LOCATION? |
| S3 | 1747534 | MEMOR? OR STORAGE? OR RAM OR SRAM OR ROM OR PROM OR EPROM - |
| | | OR EEPROM |
| S4 | 948630 | TEST? OR CHECK? OR VERIF? OR VALID? |
| S5 | 2516787 | COMPAR? OR MATCH? OR IDENTIC? OR SAME? OR DUPLICAT? |
| S6 | 4435 | (REMOV? OR REPLAC? OR REJECT? OR DISCARD?) (2N) (DUPLICAT? OR |
| | | SAME? OR IDENTICAL?) |
| S7 | 0 | S1 AND S2 AND S6 |
| S8 | 134 | S2 AND S6 |
| S9 | 134 | S8 AND (S3 OR S4 OR S5) |
| S10 | 7 | S9 AND IC=G11C? |
| S11 | 57 | S8 AND S3 AND (S4 OR S5) |
| S12 | 35 | S11 AND IC=(G06F? OR G11C?) |
| S13 | 13 | S12 AND (REDUC? OR SAVE? OR COMPACT? OR LESS OR FEWER?) |
| S14 | 17 | S12 AND (DETECT? OR FIND? OR LOCAT? OR IDENTIF?) |
| S15 | 26 | S13 OR S14 OR S10 |
| S16 | 26 | IDPAT (sorted in duplicate/non-duplicate order) |
| S17 | 26 | IDPAT (primary/non-duplicate records only) |

File 347:JAPIO Nov 1976-2004/Jan(Updated 040506)
(c) 2004 JPO & JAPIO

File 350:Derwent WPIX 1963-2004/UD,UM &UP=200432
(c) 2004 Thomson Derwent

17/5/4 (Item 4 from file: 350)
DIALOG(R) File 350: Derwent WPIX
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014727597 **Image available**
WPI Acc No: 2002-548301/200258
XRPX Acc No: N02-434085

Non-volatile memory block storing method for flash electrically erasable and programmable read-only memory identifies original and replacement data by same logical address and time stamps

Patent Assignee: SANDISK CORP (SAND-N); CONLEY K M (CONL-I)

Inventor: CONLEY K M

Number of Countries: 099 Number of Patents: 005

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|----------------|------|----------|---------------|------|----------|----------|
| WO 200258074 | A2 | 20020725 | WO 2002US366 | A | 20020107 | 200258 B |
| US 20020099904 | A1 | 20020725 | US 2001766436 | A | 20010119 | 200258 |
| EP 1352394 | A2 | 20031015 | EP 2002703078 | A | 20020107 | 200368 |
| | | | WO 2002US366 | A | 20020107 | |
| KR 2003070119 | A | 20030827 | KR 2003709551 | A | 20030718 | 200406 |
| AU 2002236723 | A1 | 20020730 | AU 2002236723 | A | 20020107 | 200427 |

Priority Applications (No Type Date): US 2001766436 A 20010119

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

WO 200258074 A2 E 31 G11C-016/00

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA
CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN
IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ
PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR
IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

US 20020099904 A1 G06F-012/02

EP 1352394 A2 E G11C-016/00 Based on patent WO 200258074

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT
LI LT LU LV MC MK NL PT RO SE SI TR

KR 2003070119 A G06F-012/02

AU 2002236723 A1 G11C-016/00 Based on patent WO 200258074

Abstract (Basic): WO 200258074 A2

NOVELTY - Method of simultaneously storing original and replacement data in non-volatile flash electrically erasable and programmable read-only memories (EEPROMs) identifies original (35) and replacement data by the same logical address and keeps track of relative times that original and replacement data were programmed into the memory.

DETAILED DESCRIPTION - Pages of non-volatile memory block are updated by programming new data (37) in unused pages of same or another block (39). Pages of new data are identified by same logical address as pages of data which they supercede and a time stamp (43) is added to note when each page was written. When reading data, the most recent pages are used and older superceded pages are ignored.

INDEPENDENT CLAIMS are included for:

(1) a method of operating a non-volatile memory system.

(2) a non-volatile memory system.

USE - In semiconductor non-volatile data storage systems, e.g. flash EEPROMs.

ADVANTAGE - The method avoids the necessity for copying unchanged data from original to new block and need to change a flag or other data in the pages of the original block whose data has been updated thereby eliminating the potential of disturbing the previously written data in adjacent pages of the same block. Keeping track of the logical offset (41') of individual pages of data within individual memory blocks, so that updated data does not have to be stored within same physical page offset as superceded data, allows more efficient use of pages of new blocks and allows the updated data to be stored in any erased pages of same block of superceded data.

DESCRIPTION OF DRAWING(S) - The drawing shows the process of
updating data of a multi-paged book. Original block (35)
New data (37))Newly assigned block (39)Time stamp (43)Logical page
offset (41')

pp; 31 DwgNo 8/16

Title Terms: NON; VOLATILE; **MEMORY** ; BLOCK; **STORAGE** ; METHOD; FLASH;
ELECTRIC; ERASE; PROGRAM; READ; **MEMORY** ; **IDENTIFY** ; ORIGINAL; REPLACE;
DATA; LOGIC; **ADDRESS** ; TIME; STAMP

Derwent Class: T01; U13; U14

International Patent Class (Main): G06F-012/02 ; G11C-016/00

File Segment: EPI

17/5/8 (Item 8 from file: 350)
DIALOG(R) File 350:Derwent WPIX
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010836641 **Image available**
WPI Acc No: 1996-333594/199633
Related WPI Acc No: 1996-041843
XRPX Acc No: N96-281184

Communication method for transferring data from mass storage device,
e.g. CD- ROM to host computer - storing separated sectors of user and
auxiliary data in contiguous memory blocks and performing error
correction on all desired sectors before transferring to host computer
via communications bus

Patent Assignee: OAK TECHNOLOGY INC (OAKT-N)
Inventor: VERINSKY P; WEDDLE G
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|------------|------|----------|-------------|------|----------|----------|
| US 5535327 | A | 19960709 | US 94264600 | A | 19940623 | 199633 B |
| | | | US 95505557 | A | 19950721 | |

Priority Applications (No Type Date): US 95505557 A 19950721; US 94264600 A
19940623

Patent Details:

| Patent No | Kind | Lan Pg | Main IPC | Filing Notes |
|------------|------|--------|-------------|--------------------------------|
| US 5535327 | A | 14 | G06F-011/10 | CIP of application US 94264600 |

Abstract (Basic): US 5535327 A

The communication method involves reading a sector of user data
from a mass storage device, e.g. a CD- ROM drive, separating the
user data from the auxiliary data and storing each portion in a
separate contiguous memory block. Error detection and correction is
performed on the data which is then labelled with a block address .

Further sectors are read and processed in the same way until all
the desired data has been transferred to memory blocks, using a
different label for each sector. The error corrected user data is then
transferred, over a communications bus, to a host computer. Pref. the
auxiliary data read from the mass storage device is stored in the
same memory block, replacing the previous auxiliary data block.

ADVANTAGE - Reduces amount of address storage required to
locate valid data blocks in DRAM. Reduces execution time required
by system controller to address each user data block.

Dwg.2/5

Title Terms: COMMUNICATE; METHOD; TRANSFER; DATA; MASS; STORAGE ; DEVICE;
CD; ROM ; HOST; COMPUTER; STORAGE ; SEPARATE; SECTOR; USER; AUXILIARY;
DATA; CONTIGUOUS; MEMORY ; BLOCK; PERFORMANCE; ERROR; CORRECT; SECTOR;
TRANSFER; HOST; COMPUTER; COMMUNICATE; BUS

Index Terms/Additional Words: COMPACT _DI SC_DRIV EB_US- 5535327 ;
DISC; DRIVE

Derwent Class: T01; T03

International Patent Class (Main): G06F-011/10

International Patent Class (Additional): G06F-003/08 ; G11B-021/10

File Segment: EPI

17/5/17 (Item 17 from File: 347)
DIALOG(R)File 347:JAPIO
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04559699 **Image available**
COMPRESSING METHOD FOR FAIL DATA AND INSPECTING METHOD FOR FAIL

PUB. NO.: 06-231599 [JP 6231599 A]
PUBLISHED: August 19, 1994 (19940819)
INVENTOR(s): SAITO TAKESHI
MARUYAMA TETSUYA
HARADA SHOICHIRO
NAKAYAMA YOSHINOBU
YOSHIDA SHINGO
KAMATA SATOSHI
SUMI YOSHIYUKI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)
HITACHI COMPUT ENG CORP LTD [472484] (A Japanese Company or
Corporation), JP (Japan)
APPL. NO.: 05-015243 [JP 9315243]
FILED: February 02, 1993 (19930202)
INTL CLASS: [5] **G11C-029/00** ; G01R-031/28; H01L-021/66
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- **Memory** Units); 42.2
(ELECTRONICS -- Solid State Components); 46.1
(INSTRUMENTATION -- Measurement); 46.2 (INSTRUMENTATION --
Testing)
JOURNAL: Section: P, Section No. 1831, Vol. 18, No. 618, Pg. 98,
November 24, 1994 (19941124)

ABSTRACT

PURPOSE: To obtain a technique for effectively compressing a fail data.

CONSTITUTION: When the redundancy of a semiconductor **memory** is relieved at a line unit containing a fail bit, a plurality of fail data 101-10n having different **addresses** on the **same** line are **replaced** with one data 20. Accordingly, unnecessary data are **reduced** in the discrimination of the propriety of redundancy relief, thus compressing fail data.

| Set | Items | Description |
|-----|---------|---|
| S1 | 614145 | FAULT? OR ERROR? OR FAIL? OF FLAW? OR DEFECT? |
| S2 | 2540835 | MEMOR? OR STORAGE? OR RAM OR ROM OR SRAM OR EPROM OR PROM - OR EEPROM OR CELL? OR ARRAY? |
| S3 | 948630 | TEST? OR CHECK? OR VERIF? OR VALID? |
| S4 | 491701 | ADDRESS? OR LOCATION? |
| S5 | 1724014 | DUPLICAT? OR MATCH? OR SAME? OR IDENTICAL? |
| S6 | 1763 | (REMOVE OR REPLAC? OR REJECT?) (2N)S5 |
| S7 | 21636 | (BIT OR WORLD) ()LINE? |
| S8 | 6714 | S1 AND S2 AND S3 AND S4 |
| S9 | 7 | S6 AND S8 |
| S10 | 17 | S6 AND S4 AND S1 |
| S11 | 66 | S2 AND S3 AND S6 |
| S12 | 18 | S11 AND (S4 OR S7) |
| S13 | 28 | S9 OR S10 OR S12 |
| S14 | 3 | S11 AND IC=G11C? |
| S15 | 28 | S13 OR S14 |
| S16 | 28 | IDPAT (sorted in duplicate/non-duplicate order) |
| S17 | 28 | IDPAT (primary/non-duplicate records only) |

File 347:JAPIO Nov 1976-2004/Jan(Updated 040506)
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File 350:Derwent WPIX 1963-2004/UD,UM &UP=200432
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| Set | Items | Description |
|-----|---------|---|
| S1 | 614145 | FAULT? OR ERROR? OR FAIL? OF FLAW? OR DEFECT? |
| S2 | 2540835 | MEMOR? OR STORAGE? OR RAM OR ROM OR SRAM OR EPROM OR PROM - |
| | | OR EEPROM OR CELL? OR ARRAY? |
| S3 | 948630 | TEST? OR CHECK? OR VERIF? OR VALID? |
| S4 | 491701 | ADDRESS? OR LOCATION? |
| S5 | 1724014 | DUPLICAT? OR MATCH? OR SAME? OR IDENTICAL? |
| S6 | 1763 | (REMOVE OR REPLAC? OR REJECT?) (2N)S5 |
| S7 | 21636 | (BIT OR WORLD) ()LINE? |
| S8 | 6714 | S1 AND S2 AND S3 AND S4 |
| S9 | 7 | S6 AND S8 |
| S10 | 17 | S6 AND S4 AND S1 |
| S11 | 66 | S2 AND S3 AND S6 |
| S12 | 18 | S11 AND (S4 OR S7) |
| S13 | 28 | S9 OR S10 OR S12 |
| S14 | 3 | S11 AND IC=G11C? |
| S15 | 28 | S13 OR S14 |
| S16 | 28 | IDPAT (sorted in duplicate/non-duplicate order) |
| S17 | 28 | IDPAT (primary/non-duplicate records only) |

File 347:JAPIO Nov 1976-2004/Jan(Updated 040506)
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File 350:Derwent WPIX 1963-2004/UD,UM &UP=200432
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17/5/20 (Item 20 from File: 350)
DIALOG(R) File 350:Derwent WPIX
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001704843

WPI Acc No: 1977-E1330Y/197720

**Dynamic memory allocation multiplexing channel - with failed main
address memory cells replaced by standby unit cells**

Patent Assignee: BURYACHENKO K K (BURY-I)

Number of Countries: 001 Number of Patents: 001

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|-----------|------|----------|-------------|------|------|----------|
| SU 526877 | A | 19760915 | | | | 197720 B |

Priority Applications (No Type Date): SU 1967237 A 19731029

Abstract (Basic): SU 526877 A

Multiplexing channel is designed for use in computing, as a digital computer data-output channel. The present model is based on a prototype with main **memory** (13), **address memory** (7) and the appropriate registers, interfaces and converters.

In order to increase the reliability of the prototype, which fails whenever both the main and **address memories** fail, and causes peripherals to fail whenever the corresponding **address memory cells**, fails, the proposed modification contains a standby **memory** unit (11).

During the operation of the unit each recording of information in the **memory** tables is followed by a readout and **address memory check**. If a **memory cell** in the **address memory** is found to have failed, it is replaced by a **cell** of the standby **memory** unit. The **address** of the corresponding peripheral is then transcribed from subchannel register (3) into a free **cell** of the associative field, and the **address** of a usable main **memory** zone is transcribed from register (9) into the corresponding **cell** of the informational field in the standby **memory** unit.

If the breakdown of the **address memory** is complete, the standby **memory** acts in the **identical** manner, **replacing** as many **cells** as its capacity permits.

Title Terms: DYNAMIC; **MEMORY** ; ALLOCATE; MULTIPLEX; CHANNEL; FAIL; MAIN;
ADDRESS ; **MEMORY** ; **CELL** ; REPLACE; STANDBY; UNIT; **CELL**

Derwent Class: T01; T04

International Patent Class (Additional): G06F-003/04

File Segment: EPI

17/5/23 (Item 23 from File: 347)
DIALOG(R) File 347:JAPIO
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04559699 **Image available**
COMPRESSING METHOD FOR FAIL DATA AND INSPECTING METHOD FOR FAIL

PUB. NO.: 06-231599 [JP 6231599 A]
PUBLISHED: August 19, 1994 (19940819)
INVENTOR(s): SAITO TAKESHI
MARUYAMA TETSUYA
HARADA SHOICHIRO
NAKAYAMA YOSHINOBU
YOSHIDA SHINGO
KAMATA SATOSHI
SUMI YOSHIYUKI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)
HITACHI COMPUT ENG CORP LTD [472484] (A Japanese Company or
Corporation), JP (Japan)
APPL. NO.: 05-015243 [JP 9315243]
FILED: February 02, 1993 (19930202)
INTL CLASS: [5] **G11C-029/00** ; G01R-031/28; H01L-021/66
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- **Memory** Units); 42.2
(ELECTRONICS -- Solid State Components); 46.1
(INSTRUMENTATION -- Measurement); 46.2 (INSTRUMENTATION --
Testing)
JOURNAL: Section: P, Section No. 1831, Vol. 18, No. 618, Pg. 98,
November 24, 1994 (19941124)

ABSTRACT

PURPOSE: To obtain a technique for effectively compressing a fail data.

CONSTITUTION: When the redundancy of a semiconductor **memory** is relieved at a line unit containing a fail bit, a plurality of fail data 101-10n having different **addresses** on the **same** line are **replaced** with one data 20. Accordingly, unnecessary data are reduced in the discrimination of the propriety of redundancy relief, thus compressing fail data.

17/5/24 (Item 24 from file: 347)
DIALOG(R) File 347:JAPIO
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03755541 **Image available**
MANAGEMENT SYSTEM FOR **MEMORY** HISTORY

PUB. NO.: 04-120641 [JP 4120641 A]
PUBLISHED: April 21, 1992 (19920421)
INVENTOR(s): IIJIMA MASANORI
APPLICANT(s): NEC IBARAKI LTD [490946] (A Japanese Company or Corporation),
JP (Japan)
APPL. NO.: 02-240672 [JP 90240672]
FILED: September 11, 1990 (19900911)
INTL CLASS: [5] G06F-012/12
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- **Memory** Units)
JOURNAL: Section: P, Section No. 1402, Vol. 16, No. 378, Pg. 28,
August 13, 1992 (19920813)

ABSTRACT

PURPOSE: To make a page having a less number of accessed times easily selectable so as to reduce the burden on a CPU and smoothly exchange pages between a main **storage** device and secondary **storage** device by storing the number of accessed times of each page.

CONSTITUTION: When a CPU reads out the contents of R bits and C bit from a page **address** (i) (i: 0-n) of a management table 1 and no data are written on the same page of a main **storage** device, necessary data are written on the same page of the main **storage** device from a secondary **storage** device. In the case the value of the C bits is other than '0', the value of the R bits is compared with a value stored in a storing section in advance and the smallest value of the R bits among the values so far **checked** is stored in the storing section. When no page having the C bits of '0' exists during the course of the operation, the operation is repeated until a page **address** (n) is completed and a certain page (with a page **address** L) of the R bits which finally remains in the storing section is **replaced** with the **same** page of the secondary **storage** device.

17/5/26 (Item 26 from file: 347)
DIALOG(R) File 347:JAPIO
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02048851 **Image available**

FAULT RECOVERY SYSTEM FOR MICROPROGRAM **MEMORY** BY SERVICE PROCESSOR

PUB. NO.: 61-262951 [JP 61262951 A]
PUBLISHED: November 20, 1986 (19861120)
INVENTOR(s): NAGASAWA TOSHIKATSU
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 60-103933 [JP 85103933]
FILED: May 17, 1985 (19850517)
INTL CLASS: [4] G06F-012/16; G06F-009/22; G06F-011/34
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- **Memory** Units); 45.1
(INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 566, Vol. 11, No. 116, Pg. 138, April
11, 1987 (19870411)

ABSTRACT

PURPOSE: To avoid a system breakdown state due to the incapability of **fault** recovery of a control **memory** by using a device processor for the correction of the **fault** of the control **memory**.

CONSTITUTION: When a parity **check** circuit 14 detects a parity **check error**, an R-SFF 15 is set through a signal line 105. Thus gates 16-18 are closed to suppress a **replacement**. At the **same** time, the trouble of a control **memory** 12 is informed to a service processor 2 through a communication control line 107. The processor 2 reads out the values of a CM register 10, a CM **address** register 11 and a CM **address** history register 13 via a scan bus 108 and **checks** te **fault** generating **address** of the **memory** 12 from the value of the register 11 to write the correct value of a microprogram command to a service processor maintenance area on the **memory** 12. While the **address** branching out to the **fault** generating **address** is **checked** from the value of the register 13 for the correction of the branch field of the microprogram command. Then the corrected field is branched out to the device processor maintenance area and written to the present **address** of the **memory** 12.

17/5/27 (Item 27 from file: 347)
DIALOG(R) File 347:JAPIO
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01189851 **Image available**
FAULT DISPOSING SYSTEM

PUB. NO.: 58-127251 [JP 58127251 A]
PUBLISHED: July 29, 1983 (19830729)
INVENTOR(s): AOYANAGI MITSUO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 57-009100 [JP 829100]
FILED: January 22, 1982 (19820122)
INTL CLASS: [3] G06F-011/00
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 232, Vol. 07, No. 241, Pg. 46,
October 26, 1983 (19831026)

ABSTRACT

PURPOSE: To facilitate an easy **fault** disposition, by reading out the contents of a buffer **memory** which holds a copy of the partial contents of a main **storage** to **check** a **fault** and holding an **address** and a reading data when a **fault** is detected and at the **same** time inhibiting **replacing** operation.

CONSTITUTION: A buffer **memory** 1 holds the partial contents of a main **storage**, and the contents of the **memory** 1 are discriminated by the **address** in the main **storage**. When the **address** of a register 3 is fed to the **memory** 1, the read-out data is transferred to a data register 2. At the same time, an **address** is transferred to an **address** buffer 4 from the register 3. The contents of the register 2 are **checked** by an **error** detector 5. If a **fault** is detected, the replacement inhibition information is delivered to a replacement inhibition line 22. Thus replacing operation for the register 2 and the buffer 4 is made incapable. The contents of the register 2 and the buffer 4 are preserved, and the data information and the **address** information are stored and preserved at a **fault** process mechanism 10. The replacement inhibition information is not delivered if no **fault** is detected at the mechanism 10.

17/5/5 (Item 5 from File: 350)
DIALOG(R)File 350:Derwent WPIX
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010895786 **Image available**
WPI Acc No: 1996-392737/199639
Related WPI Acc No: 1997-011399
XRPX Acc No: N96-330981

Programmable circuit for producing address match signal in semiconductor device - has programmable circuit storing internal address and producing address match signal and block select signal in response to address signals and internal address

Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: BERGMAN D W; CLINE D; HII F; ROUNTREE R N; WALKER D G
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 5548225 A 19960820 US 94249499 A 19940526 199639 B

Priority Applications (No Type Date): US 94249499 A 19940526

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|------------|------|-----|----|--------------|--------------|
| US 5548225 | A | | 11 | H03K-019/003 | |

Abstract (Basic): US 5548225 A

The circuit includes a first memory element, arranged for storing a datum which is an **address** bit of an array element, a second memory element, arranged for storing a first signal having first and second logic states, and a logic circuit, responsive to the datum. The first logic state and a second signal, produce an output signal having a third logic state when the datum matches the second signal. The logic circuit, responsive to the second logic state, produces the output signal having only the third logic state.

A global spare circuit (28) produces a global spare select signal, in response to the **address** match signal. A block spare circuit (34) produces a block spare select signal (BSS), in response to the global spare select signal and the block select signal.

ADVANTAGE - Produces output signal that may be used by **address match** circuit to **replace** first portion, second portion or both portions of **defective** array element, greatly increasing flexibility of spare decoder.

Dwg.1/9

Title Terms: PROGRAM; CIRCUIT; PRODUCE; **ADDRESS** ; MATCH; SIGNAL;
SEMICONDUCTOR; DEVICE; PROGRAM; CIRCUIT; STORAGE; INTERNAL; **ADDRESS** ;
PRODUCE; **ADDRESS** ; MATCH; SIGNAL; BLOCK; SELECT; SIGNAL; RESPOND;
ADDRESS ; SIGNAL; INTERNAL; **ADDRESS**

Derwent Class: U14; U21

International Patent Class (Main): H03K-019/003

File Segment: EPI

17/5/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010836641 **Image available**
WPI Acc No: 1996-333594/199633
Related WPI Acc No: 1996-041843
XRPX Acc No: N96-281184

Communication method for transferring data from mass storage device,
e.g. CD- ROM to host computer - storing separated sectors of user and
auxiliary data in contiguous memory blocks and performing error
correction on all desired sectors before transferring to host computer
via communications bus

Patent Assignee: OAK TECHNOLOGY INC (OAKT-N)
Inventor: VERINSKY P; WEDDLE G
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|------------|------|----------|-------------|------|----------|----------|
| US 5535327 | A | 19960709 | US 94264600 | A | 19940623 | 199633 B |
| | | | US 95505557 | A | 19950721 | |

Priority Applications (No Type Date): US 95505557 A 19950721; US 94264600 A
19940623

Patent Details:

| Patent No | Kind | Lan Pg | Main IPC | Filing Notes |
|------------|------|--------|-------------|--------------------------------|
| US 5535327 | A | 14 | G06F-011/10 | CIP of application US 94264600 |

Abstract (Basic): US 5535327 A

The communication method involves reading a sector of user data
from a mass **storage** device, e.g. a CD- **ROM** drive, separating the
user data from the auxiliary data and storing each portion in a
separate contiguous **memory** block. **Error** detection and correction is
performed on the data which is then labelled with a block **address** .

Further sectors are read and processed in the same way until all
the desired data has been transferred to **memory** blocks, using a
different label for each sector. The **error** corrected user data is
then transferred, over a communications bus, to a host computer. Pref.
the auxiliary data read from the mass **storage** device is stored in the
same memory block, **replacing** the previous auxiliary data block.

ADVANTAGE - Reduces amount of **address storage** required to
locate **valid** data blocks in DRAM. Reduces execution time required by
system controller to **address** each user data block.

Dwg.2/5

Title Terms: COMMUNICATE; METHOD; TRANSFER; DATA; MASS; **STORAGE** ; DEVICE;
CD; **ROM** ; HOST; COMPUTER; **STORAGE** ; SEPARATE; SECTOR; USER; AUXILIARY;
DATA; CONTIGUOUS; **MEMORY** ; BLOCK; PERFORMANCE; **ERROR** ; CORRECT; SECTOR;
TRANSFER; HOST; COMPUTER; COMMUNICATE; BUS

Index Terms/Additional Words: **COMPACT** _DI SC_DRIV EB_US- 55353 ; DISC;
DRIVE

Derwent Class: T01; T03

International Patent Class (Main): G06F-011/10

International Patent Class (Additional): G06F-003/08; G11B-021/10

File Segment: EPI

17/5/17 (Item 17 from file: 350)
DIALOG(R) File 350:Derwent WPIX
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004294254

WPI Acc No: 1985-121132/198520

XRPX Acc No: N85-090938

**Self-recovery self-monitoring microprogram control appts. - has memories
with segment state inputs connected to data inputs of segment state
registers**

Patent Assignee: TKACHEV M P (TKAC-I)

Inventor: KHARCHENKO V S; TIMONKIN G N

Number of Countries: 001 Number of Patents: 001

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|------------|------|----------|-------------|------|----------|----------|
| SU 1120337 | A | 19841023 | SU 3599402 | A | 19830603 | 198520 B |

Priority Applications (No Type Date): SU 3599402 A 19830603

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|------------|------|-----|----|----------|--------------|
| SU 1120337 | A | | 12 | | |

Abstract (Basic): SU 1120337 A

The appts. contg. **address** registers (1,16), **memories** (2,17) AND-gates (5,20), Start-Stop circuit (6) and grouped OR-gates (7), has segment state registers (3,18), AND-gates (4,9,10,12-14,19), healthy micro-instruction **storage** register (8), grouped OR-gates (11) and OR-gate (15).

The healthy microinstruction register forms micro-instructions by replacement of distorted segments and stores them until presented to the output. Information about the state of segments is stored in the other additional registers. Distorted micro-instructions are restored by **replacement** by **identical** segments of a similar micro-instruction from an opposite **memory**. Circuitry can be reshaped for non-distorted segment readout from the opposite **memory**.

USE/ADVANTAGE - In extra-reliable control of computers, stability is increased in case of failure. Each micro-instruction is divided into k segments which are **checked**. It is no longer necessary to restart a microprogram and use a truncated algorithm to perform operations..

Bul.39/23.10.84 (12pp Dwg.No.1/8)

Title Terms: SELF; RECOVER; SELF; MONITOR; MICROPROGRAM; CONTROL; APPARATUS
; **MEMORY** ; SEGMENT; STATE; INPUT; CONNECT; DATA; INPUT; SEGMENT; STATE;
REGISTER

Derwent Class: T01

International Patent Class (Additional): G06F-011/22

File Segment: EPI